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APPLICATION FOR LETTERS PATENT

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WAFER BACK SIDE COATING TO BALANCE STRESS FROM PASSIVATION LAYER ON FRONT OF WAFER AND BE USED AS A DIE ATTACH ADHESIVE

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TITLE OF THE INVENTION

WAFER BACK SIDE COATING TO BALANCE STRESS FROM PASSIVATION LAYER ON FRONT OF WAFER AND BE USED AS DIE ATTACH ADHESIVE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a divisional of application Serial No. 10/082,372, filed February 25, 2002, pending.

BACKGROUND OF THE INVENTION

[0002] Field of the Invention: The present invention relates to methods for making semiconductor dice. More specifically, the invention relates to methods and apparatus for balancing stress in a semiconductor die resulting from stress within a top side protective layer.

[0003] State of the Art: An individual integrated circuit semiconductor die is usually formed from a larger structure known as a semiconductor wafer. Wafers are usually formed by slicing a large cylindrically shaped crystal of silicon, although other materials such as gallium arsenide and indium phosphide are also used. The front side or surface of the wafer is first ground and polished to a smooth surface, for fabrication of multiple integrated circuits thereon. Each semiconductor wafer has a plurality of integrated circuits arranged in rows and columns with the periphery of each integrated circuit typically being substantially rectangular. In the electronics industry, there is a need for apparatus of smaller size, higher performance and higher memory storage. These factors drive the industry to produce smaller semiconductor dice by thinning each wafer, i.e., reducing the cross section using a mechanical and/or chemical grinding process or etching. After thinning, the wafer is sawn or diced into rectangularly shaped "dice" along two mutually perpendicular sets of parallel lines or streets separating each row and column of dice in the wafer. Thus, the individual integrated circuit semiconductor die in the form of semiconductor dice are singulated from the wafer.

[0004] Fabrication of the integrated circuits is performed on the active surface of the undivided wafer, and consists of various processes including known steps of layering, patterning, doping, etching and heat treatment, for example. Various layers applied to the active surface of

the wafer typically include insulators, semiconductors and metallic conductors. The final layering step generally comprises the application of a passivation material to cover the integrated circuit with a smooth electrically insulative protective layer. The purpose of the passivation layer is to protect the electronic components on the active surface, i.e., front side during subsequent wafer thinning, die testing, die singulation from the wafer, die packaging, and use. Exemplary passivation materials include silicon dioxide and silicon nitride (doped or undoped with boron or phosphorus, for example), as well as other materials including polymer-based compositions as known in the art. Further protection from damage during thinning of the wafer back side may be provided by temporarily attaching an adhesive-backed polymer (e.g. vinyl) sheet to the front side of the wafer. Such is disclosed in U.S. Patent 5,840,614 of Sim et al. and U.S. Patent 6,030,485 of Yamada, in which a UV sensitive tape is attached to the active surface of a wafer and made removable by radiation following back side lapping. In U.S. Patent 5,962,097 of Yamamoto et al., a protective member is removably attached to an active surface of a wafer by a pressure sensitive adhesive.

[0005] Wafer thinning is performed in order to (a) reduce the package size, (b) reduce the consumption of saw blades in subsequent die singulation from the wafer, and (c) remove any electrical junctions which have formed on the wafer back side during fabrication. The processes typically used for wafer thinning include mechanical grinding and chemical-mechanical polishing (CMP). Alternatively, etching may be used but is not generally preferred. Each of these processes requires protection of the front side or active surface of the wafer containing the electronic components of the semiconductor die and/or wafer. The wafer grinding/polishing step typically results in a somewhat rough back side which is not conducive to other semiconductor die manufacturing processes, such as direct laser marking of a semiconductor die.

[0006] Although wafer thinning produces semiconductor dice of much reduced size, it also tends to result in a higher incidence of semiconductor die breakage. In addition, stresses induced by any grinding and polishing processes must be carefully controlled to prevent wafer and semiconductor die warping or bowing. Wafer warp interferes with precise semiconductor die separation (singulation), and semiconductor die warping results in die-attach problems in subsequent packaging. In addition, warping may cause breakage of wire bonds, etc.

[0007] Stresses produced in a semiconductor die by application of a layer thereto may be classified as either "intrinsic" or result from "thermal mismatch" between the material of the semiconductor die and the material of the applied layer. In the former case, the applied layer may be in tensile or compressive stress as applied or cured. For example, a polymeric layer may shrink during a curing step to produce intrinsic compressive stress in the active surface of a semiconductor die to which it is attached. Stress resulting from thermal mismatch is particularly evident where the layer deposition is not done at room temperature. Upon cooling to ambient temperature or to a working temperature, different coefficients of expansion (CTE) result in differential contraction or expansion between the semiconductor die substrate, the wafer, and the applied layer. Each of these stress components is important in the fabrication of semiconductor die, particularly where the ratio of semiconductor die thickness to semiconductor die length (or width) is very low.

[0008] Application of an effective passivation layer to the front side of a wafer typically results in stresses in the wafer and the semiconductor die singulated therefrom. Stresses introduced by the passivation layer may be sufficient to produce undesirable warping in the semiconductor dice, particularly where the wafer has been thinned to a high degree. A rigid unwarped substrate is particularly critical in forming known-good-die (KGD) with wire bonds.

[0009] In one sawing method of singulation, the wafer back side is attached to a flexible plastic film to hold the individual semiconductor die in place during cutting. The film is subsequently separated and removed from the singulated semiconductor die, and has no effect upon die warping. In one version, the film is stretched to release the semiconductor dice, which are then simply picked off the film. The semiconductor dice may then be processed to form differing types of semiconductor packages.

[0010] In one commonly used die-attach method, an adhesive material (e.g., epoxy) is used to join the back side of a die to a carrier. The adhesive material may be insulative or be electrically conductive and heat conductive.

[0011] Layer formation on a wafer back side has been done for another purpose. Such layers have been applied to provide a smooth surface for marking a semiconductor die or wafer with indicia identifying the manufacturer, serial number, lot number, and/or bar code, for example.

[0012] Conventional laser marking techniques utilize a very high intensity beam of light to alter the surface of a semiconductor die directly by melting, burning, or ablating the device surface directly, or by discoloration or decoloration of a laser reactive coating applied to a surface of the bare semiconductor die or packaged semiconductor die. The beam of light may be scanned over the surface of the bare or packaged semiconductor die in the requisite pattern, or can be directed through a mask which projects the desired inscriptions onto the desired surface of the bare or packaged semiconductor die. The surface or coating of the semiconductor die thus modified, the laser marking creates a reflectivity difference from the rest of the surface of the semiconductor die.

[0013] Numerous methods for laser marking are known in the art. One method of laser marking involves applications where a laser beam is directed to contact the surface of a semiconductor device directly, as shown in U. S. Patents 5,357,077 to Tsuruta, 5,329,090 to Woelki et al., 4,945,204 to Nakamura et al., 4,638,144 to Latta, Jr., 4,585,931 to Duncan et al., and 4,375,025 to Carlson.

[0014] Another method of laser marking makes use of various surface coating, e.g., carbon black and zinc borate, of a different color than the underlying device material. Two examples of this type of marking are described in U.S. Patents 5,985,377 to Corbett and 4,707,722 to Folk et al.

[0015] In U.S. Patent 5,866,644 to Mercx et al., molding compounds are disclosed which form products which may be laser marked. The molding compound contains a pigment as well as glass fibers for reinforcing the molded object.

[0016] The above-indicated methods have been found to be inadequate for marking the back side of a wafer or semiconductor die, inasmuch as the thinning methods, including mechanical grinding, chemical mechanical polishing, and etching all leave the back side in a nonsmooth condition with a surface topography unsuited for laser marking (with or without a thin surface coating).

[0017] Moreover, none of the coatings, if applied to the back side of a wafer or semiconductor die, will balance wafer stress or semiconductor die stress to prevent or significantly reduce warp.

BRIEF SUMMARY OF THE INVENTION

[0018] The present invention provides a method and apparatus for balancing stresses resulting from application of a passivation layer or other layer on the front side of a semiconductor wafer. The term "passivation layer" will be used herein to denote any front side layer (compressive or tensile) which creates stress in the singulated die tending to form warp. The method and apparatus have particular application to wafers or semiconductor die which have been subjected to a thinning process, including backgrinding in particular. The present method comprises application of a stress-balancing layer (SBL) on the opposite side from a stress-creating layer such as a photoresist passivation layer, for example. Thus, a passivation layer covering the circuitry of each semiconductor die of a wafer will typically introduce compressive stresses into the dice; a stress-balancing layer (SBL) which is applied after wafer thinning but before singulation will result in individual semiconductor die in which the front side stresses and back side stresses are balanced, preventing dice warp.

[0019] The stress-balancing layer may be formed of a rigid material which resists deformation. The stress-balancing layer may be formed to have mechanical properties similar to the passivation layer and be applied under similar conditions so that the stress it creates on the die back side will approximately equal the stress on the die front side. The composition and thickness of the SBL may be varied to provide the desired balancing stress forces.

[0020] The stress-balancing layer may be applied by various methods. In a preferred method, an SBL may be applied by a chemical vapor deposition (CVD), epitaxy or other process over portions or all of the wafer back side. In particular, various CVD processes permit a uniform layer of material to be accurately deposited. Other methods which may be used to form the SBL on the back side include various evaporation methods and molecular beam epitaxy (MBE), for example.

[0021] The stress-balancing layer may comprise a composite of two or more materials. For example, semiconductor die having large aspect ratios may have formed thereon a rigid composite SBL having different reinforcing properties in the X and Y directions. Alternatively, two or more materials may be sequentially formed on the thinned wafer back side as a multilayer composite. Preferably, however, the stress-balancing layer comprises a single layer of a matrix material containing distributed particles of a reinforcing component which provide rigidity in the

X-Y plane, and more preferably, in all directions. Careful selection of materials enables the SBL to be a very thin layer which contributes little to the overall Y-dimension of a die. The stress balancing layer of this invention is generally intended to be a permanent part of a semiconductor die. An exception to this rule is when a stress-causing layer requiring an SBL is subsequently removed or its stress causing effect otherwise ameliorated, in which case the SBL may optionally be removed. Inasmuch as the SBL is a very thin layer, and its removal would weaken the semiconductor die, it is generally considered to be a permanent part of the semiconductor die. Furthermore, the SBL may serve other purposes. For example, the SBL or adhesive applied thereto may comprise a laser markable material for applying indicia to each individual semiconductor die, as discussed infra. Also, the SBL may itself comprise an adhesive material useful for bonding the die back side to a substrate such as a circuit board.

[0022] In another aspect of the invention, an adhesive layer is applied to the highly planar stress-balancing layer for back side semiconductor die attachment to a package substrate, etc.

[0023] Application of the invention results in improved ease in the manufacture of semiconductor dice, with improved semiconductor die quality (planarity and wire bonds), and concomitant reduction in defective semiconductor die.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0024] The nature of the present invention as well as other embodiments thereof may be more clearly understood by reference to the following detailed description of the invention, to the appended claims, and to the several drawings herein, wherein dimensions may be exaggerated for the sake of clarity, and wherein:

[0025] FIG. 1 is a schematic perspective view of a multidie semiconductor wafer that has been thinned and with visible die-separating streets;

[0026] FIG. 2A is a cross-sectional view of a semiconductor die with compressive stress applied thereto by a passivation layer on its front side to create die warp;

[0027] FIG. 2B is a cross-sectional view of a semiconductor die with tensile stress applied thereto by a passivation layer on its front side to create die warp;

[0028] FIGS. 3 through 10 are cross-sectional edge views of a portion of a semiconductor wafer during manufacturing processes to form semiconductor dice in accordance with the invention, wherein:

[0029] FIG. 3 is a cross-sectional view of a raw sliced wafer;

[0030] FIG. 4 is a cross-sectional view of a wafer following front side grinding and polishing;

[0031] FIG. 5 is a cross-sectional view of a wafer showing a plurality of representative electronic devices fabricated on the front side thereof;

[0032] FIG. 6 is a cross-sectional view of a wafer following deposition of a passivation layer over the electronic devices fabricated on the front side thereof;

[0033] FIG. 7 is a cross-sectional view of a wafer following back side thinning;

[0034] FIG. 8 is a cross-sectional view of a wafer following application of a stress-balancing layer on the thinned back side thereof;

[0035] FIG. 9 is a cross-sectional view of a wafer following curing of a stress-balancing layer on the thinned back side thereof;

[0036] FIG. 10 is a cross-sectional view of a semiconductor die following singulation of a wafer;

[0037] FIG. 11 is a simplified side view of a conventional backgrinding apparatus and semiconductor wafer mounted thereon;

[0038] FIG. 12 is a cross-sectional view of a wafer of the invention wherein an applied stress-balancing layer comprises a single component or a homogeneous mixture of more than one component;

[0039] FIG. 13 is a cross-sectional view of a wafer of the invention wherein an applied stress-balancing layer comprises a heterogeneous mixture of a reinforcing material in a matrix base material;

[0040] FIG. 14 is a cross-sectional view of a wafer of the invention wherein an applied stress-balancing layer comprises two separately applied sub-layers having reinforcement properties in different directions;

[0041] FIG. 15 is a cross-sectional view of a wafer following applying an adhesive layer to a stress-balancing layer on the thinned back side;

[0042] FIG. 16 is a cross-sectional view of wafer following attaching a carrier member to the stress-balancing layer in accordance with the invention;

[0043] FIG. 17A is a side view of an exemplary semiconductor die formed in accordance with the invention, illustrating a balancing of compressive stress;

[0044] FIG. 17B is a side view of another exemplary semiconductor die formed in accordance with the invention, illustrating a balancing of tensile stress; and

[0045] FIG. 18 is a view of the back side of exemplary portions of a semiconductor wafer to which three forms of a stress-balancing layer are applied in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0046] The present invention relates to semiconductor dice 20 formed in a multidie wafer 10 as shown in FIG. 1. As depicted, wafer 10 is typically circular in shape with a circumferential edge 28. The circumferential edge 28 is shown with an optional upper beveled surface 38 for ease of handling without breakage. The wafer 10 may optionally be of another shape. Semiconductor dice 20 are configured with opposing major surfaces, front side or active surface 11 and back side 12. Electronic components, not shown in this figure, are fabricated in the wafer 10 front side, i.e., active surface 11 and will be identified herein as integrated circuits. Each semiconductor die 20 of the wafer 10 is bounded by "streets" or saw lines 26 in both the X and Y directions and has an integrated circuit with bond pads thereon. The back side 12 of wafer 10 typically is free from circuitry. Following fabrication of the integrated circuits, a layer 40A (FIG. 2A) of protective passivating material is typically applied to cover the circuitry and front side surfaces.

[0047] Turning now to FIG. 2A, a side cross-sectional view of a prior art semiconductor die 20A having a thickness 92 is shown with a passivation layer 40A having a thickness 44 joined to the front side 11. Some features are exaggerated for the sake of clarity. The passivation layer 40A is shown as having laterally "shrunk" relative to the semiconductor die 20A at the extant temperature, resulting in compressive lateral stress forces16 acting at the die-layer interface 22. Reactive stress forces 18 in the semiconductor die 20A oppose the applied

stress forces forces 16, and the stress forces 16, 18 result in what is denoted herein as compressive warp.

[0048] As shown in FIG. 2B, die 20B of the prior art is shown with passivation layer 40B joined to the front side 11. The passivation layer 40B has laterally "expanded" relative to the semiconductor die 20B, creating tensile lateral stress forces 16 acting at the die-layer interface 22. Reactive stress forces 18 in semiconductor die 20B oppose the applied stress forces 16, and the result is what is denoted herein as tensile warp.

[0049] The degree of warp, whether compressive or tensile, depends upon the aspect ratio of the semiconductor die 20 and the active stress forces 16, 18. Minimization or elimination of die warp is important to the manufacture of a high quality dice with a minimum of defects.

[0050] FIGS. 3 through 10 illustrate one embodiment of the method useful for balancing stresses in semiconductor dice 20.

[0051] A portion of a semiconductor wafer 10 is depicted in FIG. 3 as comprising a wafer substrate 32. The wafer 10 has a front side 11, an opposing back side 12, and a circumferential edge 28. The wafer is sliced from a crystalline cylinder of a semiconductive material such as silicon, germanium, gallium arsenide, etc. which comprises the substrate 32.

[0052] As shown in FIG. 4, the front side 11 of the wafer 10 is ground and polished to a smooth surface which becomes the active surface of each resulting semiconductor die 20. The portion 15 of the wafer substrate material removed from the wafer 10 reduces the wafer thickness 42. This planarization step is typically conducted by chemical-mechanical polishing (CMP).

[0053] The integrated microcircuits 30 are then fabricated in accordance with a pattern on the front side (active surface) 11 of the wafer's substrate 32. As shown in FIG. 5, each microcircuit 30 is associated with a semiconductor die 20 which will be singulated along streets 26 in a later step. The microcircuit 30 typically comprises various electronic components such as transistors, diodes, resistors, capacitors, insulators, conductors, and the like, as known in the art. Typically, a series of conductive "bond pads" on the active surface permit electrical connection of the microcircuit 30 to a circuit board, a testing machine, or to the microcircuit of

another die or dice. Each microcircuit 30 is configured to provide a desired electronic result in a very small space.

[0054] Referring now to FIG. 6, it is seen that an electrically insulative passivation layer 40 is typically applied to cover the microcircuit 30 following circuit fabrication. The passivation layer 40 protects the microcircuit 30 from damage during subsequent manufacturing steps as well as in ultimate use. Unprotected, the microcircuit 30 may be degraded by contamination, chemical action, corrosion, and/or handling. Passivation layer 40 may comprise any of a variety of materials, including silicon dioxide and silicon nitride as examples. Such materials are typically applied by a chemical vapor deposition (CVP) process at elevated temperature. Thus, a difference in coefficient of thermal expansion (CTE) between the passivation layer 40 and the die material to which it is applied will result in a residual stress in the wafer 10, and in dice 20 when the wafer is diced (die singulation). For example, silicon has a CTE which is several times the CTE of silicon dioxide and will contract much more than a silicon dioxide passivation layer upon cooling from an elevated temperature, creating stress which is concentrated at the interface 22 between the wafer 10 and the passivation layer 40.

[0055] As depicted in FIG. 7, the back side 12 of the wafer 10 is then ground to reduce the thickness 42 of the wafer substrate 32. In a conventional back-grinding process, illustrated in FIG. 11, a grinding wheel 52 with grinding surface 53 grinds away a portion 25 (see FIG. 7) of semiconductor substrate material 32 from the back side surface 12. Such grinding to fully thin the wafer thickness 42 typically leaves a somewhat nonsmooth ground surface 24 with grooves and/or swirls present. However, the unevenness makes the ground surface 24 conducive to later adhesive attachment of a stress-balancing layer 50 (FIG. 8) thereto.

[0056] As shown by the arrows in FIG. 11, grinding wheel 52 of backgrinding apparatus 60 typically rotates in one direction 54 while a platen 56 providing physical support for semiconductor wafer 10 rotates in another direction 58. This results in the grinding pattern referred to above, which tends to vary from one side of wafer 10 as opposed to the other. A submount 17, formed of tape, wax, molding compound, etc., typically provides protection for the active surface 11 of the unsingulated semiconductor die 20 formed on semiconductor wafer 10 as well as structural support during the thinning process.

[0057] Turning now to FIG. 8, in accordance with this invention, a stress-balancing layer (SBL) 50 is applied to the ground surface 24 to balance the stress created by the passivation layer 40 in the wafer substrate 32. The SBL 50 is configured to adhere tightly to the ground surface 24 and to oppose warping stresses in the wafer 10 as well as in the subsequently singulated semiconductor die 20.

[0058] The stress-balancing layer 50 may be formed in a variety of ways. For example, the SBL 50 may comprise a single rigid layer or a multifilm layer with each layer formed to resist deformation in a different direction, or with different deformation properties. In another form, homogeneously distributed inorganic particles may be bound in a matrix for uniform stress resistance in an X-Y plane, or optionally, omnidirectional. The stress-balancing layer 50 may be formed of any material or materials which when applied in a thin layer to the back side semiconductor die guard surface 24, will provide a rigid structure resistant to warping of the semiconductor die.

[0059] In the event that the stress-balancing layer 50 requires a curing step to fully harden the layer, it is conducted, typically by exposure to heat or radiation (see FIG. 9)

[0060] As shown in FIG. 12, an exemplary SBL 50 is shown as a single-component highly rigid layer such as, for example, a metal, alloy, metallorganic material, a photo-resist material or other material with the proper loadbearing characteristics.

[0061] In FIG. 13, SBL 50 is shown as a heterogeneous composite structure comprising uniformly distributed strong particles in a matrix material 74. For example, very small particles of reinforcing material 72 such as metal, glass, etc. may be distributed in a matrix material of silicon oxide, silicon nitride or a polymeric material.

[0062] In a further embodiment shown in FIG. 14, two or more layers of composite materials are sequentially deposited as a stress-balancing layer 50. Each layer is shown with a reinforcing material 74A or 74B configured to resist stresses (i.e., have highest rigidity) in a particular direction, so that the layer combination provides the desired warping resistance.

[0063] Various methods may be used to deposit the materials forming the SBL 50. For example, the SBL 50 may be formed by an epitaxy process such as vapor phase epitaxy (VPE), molecular beam epitaxy (MBE), or complementary field effect transistor epitaxy (CMOSE). Sputtering and other methods may be used including physical vapor deposition (PVD).

Preferably, a chemical vapor deposition (CVD) method is used. Various CVD methods include low pressure chemical vapor deposition (LPCVD), atmospheric pressure chemical vapor deposition (APCVD), metal-organic chemical vapor deposition (MOCVD), plasma-enhanced chemical vapor deposition (PECVD), and ultra-high vacuum chemical vapor deposition (UHVCVD), any of which may be used to produce a particular stress-balancing layer 50.

[0064] The SBL 50 may itself comprise an adhesive material, particularly when combined with added reinforcement particles. For example, polymeric materials known in the art may be applied to form a rigid structure, yet retain adhesive properties. Thus, dice 20 formed therefrom may be adhesively attached to a circuit board or other substrate.

[0065] In an alternative embodiment of the present invention, an adhesive layer 48 may be applied to the stress-balancing layer 50, as depicted in FIG. 15. The adhesive layer 48 may be formed of a type of adhesive material characterized as being epoxy, or other suitable adhesive material. This adhesive layer 48 may be used as a die attach adhesive, or may be used to temporarily attach a carrier tape 62 to the wafer 10, as in FIG. 16. As discussed, infra, the adhesive layer 48 may also comprise a markable material such as a UV acrylic, thio-phene, poly-paraxylylene, (Paralene), urethanes, silicones, and acrylics, provided its strength is sufficient to resist die warping. Carrier tapes 62 are generally used to protect and hold the semiconductor dice 20 in place during sawing of the wafer 10 and enable convenient pick-off of individual semiconductor die 20 for transfer to a substrate in a semiconductor die 20 attach step.

[0066] Another embodiment of the invention utilizes a tape as a stress-balancing layer 50, wherein stresses in the plane of the tape are resisted by rigidity. The tape may be monolayer or multilayer and may be formed of or include a metal film. It is important to utilize an adhesive which will rigidly adhere to the tape and die 20 as a very thin film. The tape may be thinly adhesed on both sides, for temporary attachment to a carrier tape 62 or for permanent semiconductor die attach to a circuit board or other substrate, not shown in the figures.

[0067] Whether the stress-balancing layer 50 is applied as a tape or as a CVD layer, it may be applied to overcover the entire thinned ground surface 24, or alternatively cover selected portions of the wafer 10 or of each semiconductor die 20. For example, as shown in FIG. 18, an SBL 50 may be applied in various patterns 50X, 50Y and 50Z on the thinned semiconductor die back side 12 of each semiconductor die 20 of a wafer 10. As shown in these examples, stress-

balancing layer 50X is configured to cover the entire back side 12 as a contiguous layer. In another embodiment, the stress-balancing layer 50Y may be patterned, for example, as a continuous longitudinal strip extending over a row of semiconductor dice 20. In a further variation, stress-balancing layers 50Z are shown as discrete coverings for each individual semiconductor die. The SBL 50Z is shown as comprising a rectangular covering over a majority of a semiconductor die back side 12. However, it may comprise any pattern 68 which achieves the desired stress balancing. If applied as a tape, stress-balancing layer 50 may be applied by an automated process such that the tape is in a highly regular and standard pattern corresponding to placement on predetermined specific areas on the semiconductor dice 20, or on wafer areas which will correspond to individual semiconductor dice after singulation. As such, vision systems for reading marks on semiconductor dice can be adjusted to scan the desired marked areas. In the view of FIG. 18, the outer surface 36 of the stress-balancing layer 50X, 50Y or 50Z is uniformly planar for subsequent semiconductor die attach.

[0068] Although the stress-balancing layer 50 may be sometimes usefully applied to already singulated die 20, it is preferred to apply stress-balancing layer 50 to the wafer ground surface 24 prior to singulation, because this avoids warpage resulting from singulation and is generally more cost-effective.

[0069] Exemplary semiconductor dice 20C and 20D formed by the method of the invention are illustrated in FIGS. 17A and 17B. As illustrated in FIG. 17A and 17B, a stress-balancing layer 50C or 50D is applied to the back side 12 of a semiconductor die 20C, 20D, respectively. This layer 50C or 50D balances stress forces 18 in die 20C or 20D caused by compressive or tensile stress forces 16 in passivation layer 40C and 40D, and maintain the semiconductor dice in a generally warp-free condition. The counter forces 70 in the SBL 50C, 50D balance the warping forces 16 in the passivation layer 40C, 40D.

[0070] The SBL 50 is particularly useful when it, or an adhesive layer 48 applied thereto, is configured to be used as an indicia marking layer. FIG. 19 illustrates in a simplified schematic view of a conventional laser marking system 100 capable of readily marking semiconductor dice 20 to which a laser markable material has been applied. The system 100 comprises a laser 102, a lens system 104, a shadow mask 106 and a laser control system 108 for monitoring and controlling the function of the apparatus. For purposes of this invention, a

"laser" is considered to be any optical energy source capable of marking a surface of a stress-balancing layer 50 through the use of light energy and/or heat. Preferably, laser 102 is comprised of an Nd:YAG (yttrium aluminum garnet), Nd:YLP (pulsed yttrium fiber laser), carbon dioxide, or other suitable optical energy devices known in the art. It is understood, however, that laser 102 may also comprise an ultraviolet (UV) energy source or other energy beam. When laser 102 is energized, an intense beam of light 115 is projected from lens system 104 through shadow mask 106 onto the surface of the laser markable material (SBL 50 or adhesive 48 applied thereto). When laser beam 115 impinges on laser markable material 50, 48, the material in, on, embedded in, attached to or under the material is altered, e.g., by heating, vaporization, burning, melting, chemical reaction, residue or dye transfer, or combinations thereof. The result comprises a color or texture change, or both, having an image of shadow mask 106 appearing on the ground surface 24 of the semiconductor die 20. Although a shadow mask 106 is shown in this embodiment, the present invention contemplates computer-directed operation, including mechanical movement of laser 102 in conjunction with, or without, shadow mask 106.

[0071] The stress-balancing layer 50 may advantageously be formed of a material which also has antistatic properties.

[0072] The present invention is applicable to semiconductor dice of any electronic or physical configuration, in which stresses tending to warp the semiconductor dice are present. Thus, for example, the semiconductor die may be one of a DIP, SIP, ZIP, PLCC, SOJ, SIMM, DIMM, LCC, QFP, SOP, TSOP, flip-chip, etc.

[0073] Thus, in the present invention, a layer 50 may be formed on the ground surface 24 of a semiconductor wafer 10 to balance warping stresses in the subsequently singulated semiconductor dice 20. In addition, the layer 50 may be configured to be or support a markable layer on the die's thinned ground surface 24. The layer 50 may also be configured to comprise or support a semiconductor die attach adhesive or carrier adhesive.

[0074] The stress-balancing layer 50 which is applied to the back side 12, 24 of a thinned wafer 10 may comprise only a very small portion of the Z dimension of the subsequently singulated dice. The thickness 42 of the SBL 50 will depend upon the footprint size and thickness of the die and will generally be larger as the footprint increases. Typically, for the stresses normally encountered in small semiconductor dice 20, i.e., less than about 10 mm in the

X and Y dimensions and less than about 1.5 mm in the Z dimension, the thickness 42 of the SBL 50 is generally less than about 0.1 mm and effectively prevents or counteracts the tendency to warp. The SBL 50 may be formed of the same material as the stress-causing passivation layer 40 and be of a similar thickness 42.

[0075] While the present invention has been disclosed herein in terms of certain exemplary embodiments, those of ordinary skill in the art will recognize and appreciate that it is not so limited. Various combinations or modifications to the disclosed embodiments may be effected without departing from the scope of the invention. Moreover, features from one embodiment may be combined with features from other embodiments.

[0076] For example, this invention, while being described with reference to semiconductor wafers containing integrated circuits and individual semiconductor dice, has equal utility to any type of substrate in which compressive or tensile stresses require balancing. Furthermore, the invention finds added utility where two or more of stress balancing, marking, adhesion, and surface protection of a substrate are desired to be simultaneously achieved. The scope of the instant invention is only to be limited by the claims which follow and equivalents thereof.